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1. **µC-based signal processing in process monitoring**
Petuelli, G.; Blum, G.; Schmitte, F.-J.; Welkner, K.;
AFRICON, 1999 IEEE
Volume 1, 28 Sept.-1 Oct. 1999 Page(s):501 - 506 vol.1
Digital Object Identifier 10.1109/AFRCON.1999.820933
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Frequency/phase locked loop clock synthesizer using an all digital ...
The **digital loop** includes an all digital **frequency difference detector** (FDD), which controls the center frequency of the **VCO**. The **analog loop** includes an **...**
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VCO. X. s(t). e(t). v(t). Figure 3.1: Simple illustrative **PLL** model. = −cos(ω **...** phase detector (PD) with a **frequency difference detector** (FDD). **...**
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File Format: PDF/Adobe Acrobat
A **PLL** with a **digital loop** filter is explored. The main advantage of the DPLL is that it avoids ... phase error by a high frequency clock, such as the **VCO**. ...
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the high-speed BBPLLs implemented up to now use **analog loop**. filters, we extend the concept and ... analog LC **VCO**. The frequency resolution of the DCO goes ...
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Direct digital frequency synthesis enabling spur elimination ...
... into a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage controlled oscillator (**VCO**). In FIG. ...
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Hybrid phase-locked loop employing analog and **digital loop** filters ...
a **digital loop** filter coupled to the phase-**frequency detector** including a ... The **VCO** 130 is an analog device. Consequently, the **PLL** 110 can achieve a high ...
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[PDF] A DIGITALLY PROPULSIVE **PLL** FOR TIMING RECOVERY APPLICATIONS
File Format: PDF/Adobe Acrobat - View as HTML
analog loop, acting as in a conventional **PLL**, locks to the. input phase difference. ...
Phase-**Frequency detector** facilitates the **digital loop** to ...
iris.elf.stuba.sk/JEEEC/data/pdf/07-08_105-7.pdf - Similar pages

[PDF] A Compact, Low-Power Low-Jitter Digital **PLL**
File Format: PDF/Adobe Acrobat - View as HTML
1. A **PLL** consists of five main blocks: a phase-. **frequency detector** (PFD), a charge pump, a loop filter ... A **PLL** with a **digital loop** filter is explored. ...
www.imec.be/esscirc/essderc-esscirc-2003/papers/all/578.pdf - Similar pages

[PDF] Event-Driven Modeling and Simulation of an Digital **PLL**
File Format: PDF/Adobe Acrobat - View as HTML
Listing 6 shows the model of the **digital loop** filter,. 1. 1. UP. DN. T2D. Fref. Fref. PFDout. DFF. DFF. Figure 4. The digital phase and **frequency detector** ...
www.bmas-conf.org/2006/3.2_paper.pdf - Similar pages

Digital phase-locked loop - US Patent 6970046
This analog phase-locked loop comprises a phase/**frequency detector** (PFD), ... the **analog loop** filter can be replaced by any desired type of a **digital loop** ...
www.patentstorm.us/patents/6970046-description.html - 39k - Cached - Similar pages

Compact phase recovery scheme using digital circuits - US Patent ...
Prior art designs which implement an **analog loop** filter use at least one discrete ... The **PLL** uses a voltage controlled oscillator (**VCO**) in which the output ...

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[PDF] Phase-Locked Loops: A Control Centric Tutorial
File Format: PDF/Adobe Acrobat - View as HTML
VCO as integrator makes every **PLL** at least Type 1 ... The combination of a tri-state phase-**frequency detector** and a charge pump. ... **Analog Loop** Filters ...
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"frequency detector" AND "digital loop" AND "analog lc Search

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☐ **1.** Integrated RF building blocks for base station applications [PDF-273K]
Jan 2003
...chips including all building blocks of a **PLL**-based synthesizer except for the voltage...One of the main problems of the integer-N **PLL** based synthesizer when used in a multichannel...Kostamovaara J (1998) A Bipolar Semicustom **PLL** Based Synthesizer for GSM and DCS Systems...
[http://herkules.oulu.fi/isbn951426908X/isbn951426908X....]
similar results

☐ **2.** AN INVESTIGATION OF CARRIER RECOVERY [PDF-215K]
Oct 1998
...error detector of some sort, which for the **PLL** is a PD, modeled in Figure 3.1 as a multiplier, 2) a loop filter, and 3) a **VCO**. Note that for an AFC loop the error term...THE PHASE-LOCKED LOOP 13 Loop Filter **VCO** X s(t) e(t) v(t) Figure 3.1: Simple illustrative **PLL** model = - cos(ct +) · sin(ct...design progresses. 3.2 Linearized Analog **PLL** Model Assuming that after some convergence...phase domain model of Figure 3.2 where the **VCO** is modeled as a perfect integrator with...
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☐ **5.** DIRECT DIGITAL FREQUENCY SYNTHESIS ENABLING SPUR ELIMINATION
SANDER, Brian / SANDER, Wendell, *PATENT COOPERATION TREATY APPLICATION*,

Sep 2000
...a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage...controlled oscillator (**VCO**). In Figure 3...controlled oscillator (**VCO**). Finally, an output of the **VCO** is input to the...As compared to a **PLL** using a conventional phase/**frequency detector** (PFD), the **PLL**...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **6.** Direct digital frequency synthesis enabling spur elimination
Sander, Wendell / Sander, Brian, *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Jul 2000
...voltage-controlled oscillator (**VCO**). Finally, an output of the **VCO** is input to the...As compared to a **PLL** using a conventional phase/**frequency detector** (PFD), the **PLL**...a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage...controlled oscillator (**VCO**). In FIG. 3, the...
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☐ **7.** DIRECT DIGITAL FREQUENCY SYNTHESIS ENABLING SPUR ELIMINATION
SANDER, Brian / SANDER, Wendell, *EUROPEAN PATENT*, Jun 2002
...a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage...controlled oscillator (**VCO**). In Figure 3...controlled oscillator (**VCO**). Finally, an output of the **VCO** is input to the...As compared to a **PLL** using a conventional phase/**frequency detector** (PFD), the **PLL**...
Full text available at patent office. For more in-depth searching go to LexisNexis
view all 8 results from Patent Offices
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☐ **8.** Phase locked loop using digital loop filter and digitally controlled oscillator
May, Michael R. / Cave, Michael D., *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Mar 1998
...Phase-Locked Loops (**PLL**) are one type of oscillator...and memory devices. **PLL**'s synchronize output...controlled oscillator (**VCO**) synchronizing clock...block diagram of a **digital loop** filter illustrated...provides as input to the **digital loop** filter 12. The RANDOM...A Type IV phase and **frequency detector** 21 connects to a D...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **9.** Modulation and frequency synthesis for wireless digital radio
Bax, Walter T., Jan 2000
...120 4.2.3 Phase-**Frequency Detector**...4.37 Phase-**frequency detector** with asynchronous reset 130...132 4.10 Differential phase-**frequency detector** transfer function...
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☐ **10.** Timing control for PRML class IV sampling data detection channel
Johnson, Kenneth E. / Abbott, William L. / Nguyen, Hung C., *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Nov 1993
...controlled oscillator (**VCO**). Logic gating at...transition edges. The **PLL** operating frequency...PR4,ML system, a **PLL** has been needed...Separate phase/**frequency detector** circuits must be...selected to control the **PLL** oscillator frequency...approach, a common **analog loop** compensation filter...facilitate the use of a **digital loop** filter during READ...
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☐ **11.** An Investigation of Carrier Recovery Techniques for PSK Modulated Signals in CDMA and Mulipath Mobile Environments
Nicoloso, Steven P., May 1997
...12 3.2 Linearized Analog **PLL** Model . . . . . 13 3.2.1 The Second-Order **PLL** . . . . . 14 3.2.2 The Third-Order **PLL**...
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☐ **12.** Zero phase start optimization using mean squared error in a PRML recording channel
Ziperovich, Pablo A. / Chiao, James, *EUROPEAN PATENT APPLICATION*, Mar 1996
...a phase locked loop ("**PLL**") to generate a coherent...mode is entered, the **PLL**, typically acquires the...controlled oscillator ("**VCO**") has had an ENABLE input...output by the timing loop **VCO** coincided at the input to the phase-**frequency detector** simultaneously, or nearly...error was near zero, and **PLL** acquisition time was...
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☐ **13.** An investigation of carrier recovery techniques for PSK modulated signals in CDMA and mulipath mobile environments
Nicoloso, Steven P., Jan 1997
...12 3.2 Linearized Analog **PLL** Model . . . . . 13 3.2.1 The Second-Order **PLL** . . . . . 14 3.2.2 The Third-Order **PLL**...
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☐ **14.** Zero phase start optimization using mean squared error in a PRML recording channel
Ziperovich, Pablo A. / Chiao, James, *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Sep 1996
...charge pump 270 passes into an **analog loop** low pass filter 274. The loop...analog charge pump 270 and the **analog loop** filter 274. Thus, during non-read...detector 268, charge pump 270, **analog loop** filter 274 and buffer 260...the frequency synthesizer **PLL** 262. Ordinarily, the timing...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **15.** Digital filtering, data rate conversion and modem design
Terrell, Peter M., *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Mar 1996
A digital filter 23 receives a control signal which specifies what filter coefficient values should be used. The control signal can be changed repeatedly so as to dynamically select the coefficients in response to the value of a control parameter. The ...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **16.** AN INVESTIGATION OF CARRIER RECOVERY [PDF-244K]
Oct 1998
...Example of a feedback control system: A simple **PLL** model . . . . . 6 1.3 Example open-loop...7 3.1 Simple illustrative **PLL** model...13 3.2 Linearized, phase domain model of **PLL**...
[http://scholar.lib.vt.edu/theses/available/etd-1133179...]
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17. AN INVESTIGATION OF CARRIER RECOVERY [PDF-316K]

☐ Jun 1997
...submit. v 3.6 The Notion of Optimality for a **PLL**...Example of a feedback control system: A simple **PLL** model . . . . . 6 1.3 Example open-loop...7 3.1 Simple illustrative **PLL** model...
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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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1. **Determination of intensity correlation functions from photoelectric count**
Meltzer, D.; Mandel, L.;
Quantum Electronics, IEEE Journal of
Volume 6, Issue 11, Nov 1970 Page(s):661 - 668
Abstract | Full Text: PDF(872 KB) IEEE JNL
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2. **Authors' Reply[2]**
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Computers, IEEE Transactions on
Volume C-20, Issue 12, Dec. 1971 Page(s):1617 - 1617
Abstract | Full Text: PDF(248 KB) IEEE JNL
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3. **A Simplified Definition of Walsh Functions**
Lackey, R.B.; Meltzer, D.;
Computers, IEEE Transactions on
Volume C-20, Issue 2, Feb. 1971 Page(s):211 - 213
Abstract | Full Text: PDF(576 KB) IEEE JNL
Rights and Permissions

4. **A 1.0-GHz single-issue 64-bit powerPC integer processor**
Silberman, J.; Aoki, N.; Boerstler, D.; Burns, J.L.; Sang Dhong; Essbaum, A.; C
Heidel, D.; Hofstee, P.; Kyung Tek Lee; Meltzer, D.; Hung Ngo; Nowka, K.; Po
Takahashi, O.; Vo, I.; Zoric, B.;
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Digital Object Identifier 10.1109/4.726542
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5. **Designing for a gigahertz [guTS integer processor]**
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S.D.; Takahashi, O.;
Micro, IEEE
Volume 18, Issue 3, May-June 1998 Page(s):66 - 74
Digital Object Identifier 10.1109/40.683106

Abstract | Full Text: PDF(308 KB) IEEE JNL
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6. **"Timing closure by design," a high frequency microprocessor design me**
Posluszny, S.; Aoki, N.; Boerstler, D.; Coulman, P.; Dhong, S.; Flachs, B.; Hofs
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7. **Clocking strategies and scannable latches for low power applications**
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8. **A 1 GHz single-issue 64 b PowerPC processor**
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Lee, K.; Meltzer, D.; Nowka, K.; Park, J.; Peter, J.; Posluszny, S.; Shapiro, M.;
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Posluszny, S.; Aoki, N.; Boerstler, D.; Burns, J.; Dhong, S.; Ghoshal, U.; Hofst
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11. **A 1.0 GHz single-issue 64 b powerPC integer processor**
Silberman, J.; Aoki, N.; Boerstler, D.; Burns, J.; Dhong, S.; Essbaum, A.; Ghos
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1. **Noise analysis of phase-locked loops**
Mehrotra, A.;
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2. **A CMOS monolithic ΔΣ-controlled fractional-N frequency synthesizer for**
De Muer, B.; Steyaert, M.S.J.;
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Kamal, M.M.; El-Shewekh, E.W.; El-Saba, M.H.;
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6. **CMOS wide-swing differential VCO for fully integrated fast PLL**
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8. **A frequency hopping synthesizer chip for GSM and DCS systems**
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12. **A 2.5 to 10GHz clock multiplier unit with 0.22ps RMS jitter in a 0.18/spl m technology**
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Hansen, F.; Salama, C.A.T.;
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